Shop Floor Scheduling of Semiconductor Wafer Manufacturing

By

Mauricio Guilherme De Carvalho Resende

Engineer (Catholic University of Rio de Janeiro) 1978
M.S. (Georgia Institute of Technology) 1979

DISSERTATION

Submitted in partial satisfaction of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

ENGINEERING

in the

GRADUATE DIVISION

OF THE

UNIVERSITY OF CALIFORNIA, BERKELEY

Approved: Roger Glassey 13 Aug. 87
Chairman Date

Robert C. Leachman 13 Aug 87

David A. Hodges 13 August 1987

DOCTORAL DEGREE CONFERRED
DECEMBER 15, 1987

Shop Floor Scheduling of Semiconductor Wafer Manufacturing

Mauricio Guilherme de Carvalho Resende

Shop Floor Scheduling of Semiconductor Wafer Manufacturing

Mauricio G.C. Resende

Doctor of Philosophy — Industrial Engineering and Operations Research

---

C. Roger Glassey
Chairman of Committee

Abstract

Semiconductor wafer fabrication is perhaps the most complex manufacturing process found today, with a wide range of complex issues related to production planning and scheduling. Computer-integrated manufacturing (CIM) systems make it possible, in theory, to use global factory state information for factory control decisions. The possibility of making decisions on an expanded information set raises two of the research question treated in this dissertation: How should global information be summarized and used for decisions and how much improvement can one expect as a result, compared with decisions based on local information?

This research investigates lot release control and dispatching policies for shop-level scheduling of a semiconductor fab. We introduce a closed-loop scheduling policy, called Starvation Avoidance, that makes use of global factory state information and that in simulation experiments compares favorably to traditional scheduling policies (that use local and global information) with respect to the tradeoff between

throughput and queueing time.

The virtual inventory of the bottleneck resource is defined to be the work content at the bottleneck of all jobs either at the bottleneck station or expected to arrive at the bottleneck within a given lead time. Starvation avoidance monitors the virtual inventory and controls work release to avoid idling bottleneck machines without overloading the bottleneck.

The plan for the dissertation is as follows. Chapter 1 introduces the problem. In Chapter 2 we discuss at a superficial level the processes involved in transforming a slice of raw silicon into a wafer of integrated circuits. In Chapter 3 we review the literature of job shop scheduling (in particular, job shop dispatching) and scheduling and simulation of semiconductor wafer manufacturing. In Chapter 4 we introduce a queueing model of the dynamics of a semiconductor wafer fab and present a C programming language implementation of the model. In Chapter 5 we introduce a class of new job release mechanisms called Starvation Avoidance (SA). In Chapter 6 we compare several dispatching rules and release strategies on hypothetical and real data. Concluding remarks are made in Chapter 7.

For

Lucia

Acknowledgement

The development of this dissertation would not have been possible without the four and a half years of financial support from my Brazilian sponsoring agency, Conselho Nacional de Desenvolvimento Científico e Tecnológico – CNPq. Research in Computer Integrated Manufacturing at Berkeley is supported by the Semiconductor Research Corporation, Fairchild Semiconductor Corporation, Philips Research Laboratories, and The State of California through *Project MICRO* – Microelectronics Innovation and Computer Research Opportunities. Cray Research provided financial support for computer time on the Cray X-MP/14 supercomputer at U.C. – Berkeley.

During my five years as a graduate student at Berkeley, I learned much from Professor Ilan Adler. Our research on the implementation of Karmarkar's algorithm for linear programming brought many moments of excitement and intellectual fulfillment. Professor Richard E. Barlow introduced me to network reliability and encouraged me to publish my first paper in a U.S. scientific journal. It was an honor to have been a student of Professors Adler and Barlow.

Professor David A. Hodges introduced me to the problem of scheduling semiconductor manufacturing and to computer integrated manufacturing in general. Without his drive, this research could not have taken place. Professor Robert C. Leachman gave me constant encouragement by always demonstrating interest in my research. I thank them both for having participated in my dissertation committee.

Above all, I would like to express my thanks to Professor C. Roger Glassey. As an effective advisor, he guided my way through the many phases of scientific discovery and production. It has been both a pleasure and a challenge to work under his supervision.

To my many friends and colleagues at Berkeley, I thank you all for having made these years enjoyable. I will miss you all.

Randy Hughes and Don Ruffcorn at Schlumberger Palo Alto Research – Fairchild influenced my work by helping me see some *real* scheduling problems in industry.

I thank my Mother and Father for their loving support and encouragement during my *many, many* years as a student.

Finally, I thank Lucia for being my permanent source of love and strength.

Table of Contents