Chapter 2 — Integrated Circuit Fabrication

The worldwide integrated circuit (IC) market is expected to reach yearly sales in the order of $100 billion by 1990 [Ano81a, Ano82a, Ano82b] up from approximately $1 billion in 1970. This volume will be comparable to that of the automobile, chemical, and steel industries [Sze83a]. The foremost economic goal of the semiconductor device industry is the reduction of development and manufacturing costs per chip [Old77a]. To achieve the goal of economies of scale, circuit manufacturers must reduce device dimensions, increase the number of devices produced on a wafer, increase the number of wafers batched together, and increase the number of lots that can be processed simultaneously. In this way a large number of circuits can share the cost of labor and equipment. This, in fact, has occurred in the last 25 years, when component dimensions have shrunk exponentially while the number of components per chip has experienced exponential growth [Moo80a]. Today, chips are commercially available with minimum feature lengths in the sub-1 μm range and with over 1 million components. Consequently, an exponential decrease has occurred in the cost per bit in RAM chips [Noy81a].

Manufacturers must aim continuously to increase *yield*, *i.e.*, the proportion of good chips produced on wafer. Yields tend to increase as device size decreases [Old77a] and as processes mature, but yields of less than 30 percent for mature processes are commonly found in industry today. Equipment required for manufacturing semiconductor devices is costly. Prices in the over $1 million range are not uncommon. Efficient utilization of expensive equipment is therefore an important goal for manufacturers.

The semiconductor industry has not kept pace with other industries (such as automotive, petro-chemical, and steel) with regards to production planning and scheduling [Gar84a]. Production processes must be simplified and production logistics improved.

In this Chapter we describe the semiconductor fabrication process. We begin by presenting a brief overview of the IC fabrication process. We are far from complete in our description, limiting ourselves only to a level of detail that suffices for understanding the shop-level scheduling problems involved.

2.1 — Integrated Circuits

Integrated circuits are intricate three-dimensional structures with a complex internal composition built on wafers of semiconductor material. Silicon-based ICs account for 98% of all semiconductor devices sold worldwide [Sze83a]. We limit our exposition to silicon-based devices. As mentioned earlier, our discussion of IC fabrication is limited to an introductory level. For a detailed exposition of the subject, the reader is referred to Oldham [Old77a], Gise and Blanchard [Gis79a, Gis86a], and Sze [Sze83a].

The IC manufacturing process begins with the production of wafers. Raw wafers are usually produced by third parties and when purchased are ready for processing. Very pure single-crystal silicon is grown from specially pure sand (silicon dioxide). If required, the crystal is ground into a perfect cylindrical shape. Millimeter-thin slices, called raw wafers, are sawed from the crystal, polished, and shipped to IC manufacturers.

In fabrication, three dimensional structures are defined on the silicon wafer. After fabrication, wafers are probed and defective dice are marked. Wafers are then sectioned into tens to hundreds of chips. These are sorted according to performance characteristics, assembled in protective shells, further tested and sorted and finally shipped.

In this research we do not consider production problems that arise in the pre- and post-fabrication phases of circuit manufacturing, but rather limit ourselves to fabrication. See Gise and Blanchard [Gis79a, Gis86a] and Sze [Sze83a] for a discus-

sion of both wafer preparation and the post-fabrication phases of integrated circuit manufacturing. See Leachman [Lea86a] for a corporate-level production model of semiconductor manufacturing.

The IC fabrication process takes place in a clean room, where special measures are adopted to maintain the level of particle contamination low. Circuits are constructed in layers, one at a time. Each layer is defined by a pattern on a glass plate, called a photomask, whose features are transferred to the surface of the silicon wafer. This process of photo-engraving, called photolithography or simply masking, is key to fabrication. A wafer commonly undergoes over ten photolithographic steps in its fabrication process.

Between visits to the photolithography station a wafer visits stations where other physical and chemical processes are carried out. These include oxidation, diffusion, ion implantation, metallization, and etching. The fabrication process may require over 10 weeks from raw wafer to wafer probe. It can be viewed as follows.

```
begin process
    for k = 1 to number_layers do
        grow or deposit k-th layer

        begin photolithography
            apply photoresist
            pre-bake oven
            with k-th mask align and expose
            develop, rinse and dry
            post-bake oven
            inspect and measure
        end

        etch
        introduce impurities
        strip resist
    end
end.
```

In the remainder of this Chapter we describe in more detail each of the main processes encountered in semiconductor wafer fabrication.

2.1.1 – Deposition and Epitaxy

As each level of the wafer is defined a thin layer of material must be grown or deposited on the wafer surface to provide conducting regions within the device, protection from the environment, and electrical insulation between metals. The most common techniques for deposition are atmospheric presure chemical vapor deposition (CVD), low-presure chemical vapor deposition (LPCVD), and plasma-assisted chemical vapor deposition (PCVD).

In chemical vapor deposition, the wafer and gaseous compounds react thermally in a reaction chamber, producing a thin layer of a desired stable compound on the surface of the wafer. This is usually a batch operation with several lots processed in parallel. Reaction chambers (furnaces) vary much in type, *e.g.* horizontal, vertical, cylindrical, and gas-blanketed down-flow systems. The most commonly deposited materials include polycrystalline silicon, silicon dioxide (doped and undoped), and silicon nitride.

Epitaxial deposition is a special form of CVD, its special characteristic being that a thin *crystalline* film is deposited on the wafer surface. Several techniques have been developed for epitaxial deposition, including vapor growth, hydrogen reduction of silicon tetrachloride, and pyrolysis of silane. The deposition process begins by cleaning the wafer surface. The wafers are loaded on the epitaxial system with great care so as not to contaminate their surfaces. The epitaxial system is heated up to the proper temperature and a thin region of damaged silicon is removed from the surface of the wafer by means of an HCl etch. In the deposition step the layer is actually grown and doped. Finally the system is cooled down and the wafers are unloaded.

A more recent technology for epitaxial deposition is molecular beam epitaxy.

This process is carried out in a hard vacuum and as a result there is less diffusion of doped impurities than with furnace-based epitaxy.

2.1.2 – Oxidation

In the process of oxidation, a protective layer of silicon dioxide is grown on the surface of the silicon wafer. Oxidation is required throughout the entire IC fabrication process. Silicon dioxide has several uses [Sze83a]: to act as a mask against implant or diffusion of dopant into silicon; to provide surface passivation so that wafers do not degrade when exposed to air [Loz86a]; to isolate one device from another; and to serve as a component in MOS structures. The ability to grow such a layer makes silicon one of the most used semiconductor materials. Techniques for producing silicon dioxide include thermal oxidation, wet anodization, chemical vapor deposition, and plasma anodization or oxidation, the most common of which is thermal oxidation.

Thermal oxidation takes place in an oxidation furnace. It is a batch operation where several lots are processed simultaneously. Wafers are exposed to an atmosphere of O_2 or water vapor at temperatures in the 900–1300°C range. Oxidation is preceded by a cleaning operation designed to remove any impurities that may be present on the wafer surface. After cleaning, the wafers are dried and placed on a holder to be loaded on the furnace. The thickness of the oxide grown on the wafer surface is proportional to the furnace temperature and the length of exposure.

2.1.3 – Introduction of Impurities

Certain portions of the wafer require the introduction of controlled amounts of selected impurities. Two technologies are used for achieving this goal: diffusion and ion implantation. Diffusion takes place in a furnace and requires a pre-clean operation. In predeposition, the first step of the two step diffusion procedure, a carefully controlled amount of impurity is introduced into the wafer. Wafers are exposed, in batch, to a gaseous ambient of the dopant. By controlling temperature and time of

exposure the correct amount of impurities can be introduced. Another technique for predeposition makes use of source wafers, *i.e.* wafers made of the dopant material. Device wafers and source wafers are arranged next to each other and placed together in the furnace. The second step of diffusion is called drive-in. In this step no dopant is further introduced into the wafer, but rather the already introduced dopant is driven into the wafer to a desired depth. Diffusion is a batch operation.

In ion implantation, an electrical field accelerates ions of the desired dopant into the semiconductor. By scanning the wafer, a uniform predeposition can be obtained. The depth of deposition is controlled by the energy used to accelerate the particles. Ion implantation is performed one wafer at a time, with doses requiring anywhere from 5 seconds to 15 minutes of exposure. Following implantation, the wafer is often placed in a high-temperature furnace called a rapid thermal annealer to correct any damage caused by the implanter to the crystalline structure of the substrate.

2.1.4 — Photolithography

Photolithography, or masking, is central to semiconductor component manufacturing. It is in this step that circuit geometries are defined. Photomasks, containing the image to be transferred to the wafer are usually produced, under contract, by third parties. At the fabrication facility they are maintained in a mask library at the masking station. The mask generation process is a complex engineering task that is beyond the scope of this thesis. It is in the photolithography station that one finds the most costly processing equipment. For this reason and because process recipes require wafers to frequently return to photolithography, photomasking is commonly the bottleneck work station.

Gise and Blanchard [Gis79a] divide the photolithography process into eleven steps:

- substrate preparation

- surface preparation
- application of resist
- soft bake
- align and expose
- visual inspection - develop check
- hard bake
- etch
- strip resist
- final visual inspection

A substrate is grown on the surface of the wafer. This usually involves an oxidation step, but may also require a chemical vapor deposition (CVD), or a diffusion step.

In some instances the surface of the wafer must be cleaned prior to the application of the photoresist. Photoresist is a substance that is sensitive to ultra-violet (UV) radiation but not to the yellow light that illuminates the station. Light-hardened, or negative, resist hardens when exposed to UV radiation, while light-softened, or positive, resist softens. Resist is applied on the wafer by using a spinner. A spinner is a rapidly rotating devise on which the wafer is placed. A controlled amount of liquid photoresist is placed in the center of the spinning wafer and moves outward evenly on the wafer surface. This requires approximately 30 seconds and is done one wafer at a time.

In soft bake, or pre-bake, any extra solvent is baked out of the resist and the adherence of the resist to the wafer is increased. Soft bake is either carried out with hot air or infrared radiation. After cooling, the wafer moves to the most sensitive operation in the fabrication process — align/expose.

The photomask and wafer are brought tightly together, sometimes making use of vacuum to achieve bondness, and the mask is aligned to any previously defined

pattern on the wafer. First layer photolithography does not require alignment. After alignment has been achieved the mask and wafer are exposed to UV radiation, which reacts with the unprotected portion of the photoresist. Sze [Sze83a] estimates that in an industrial setting align/exposers can process approximately 100 wafers per hour. Aligners are characteristically unreliable and frequently go down for repair [Loz86a]. The softened part of the resist is dissolved and removed in the develop step.

The wafer is tested for proper alignment and resist quality and if approved is sent to hard bake. In hard bake more solvents are evaporated and the bond of the resist to the wafer surface is increased to withstand the subsequent etching processes. The equipment and baking times for hard bake are usually the same as for soft bake, but temperatures are higher.

The next step is etching. Two technologies exist for etching -- wet and dry etching. Wet etching takes place in a wet sink where a wafer lot is submerged in a bath of acid at a specified temperature. The acid selectively attacks portions of the wafer not protected by the hardened resist. After etching, wafers are washed and dried on a spinner dryer. In dry etching, or plasma etching, the wafer is placed in a chamber filled with a reactive gas. A magnetic field is applied to the gas, which etches away unprotected areas of the top layer. Dry etching produces sharper resolution than wet etching, where chemicals may undercut the resist.

Finally the resist is removed by either an acid bath or plasma techniques and the wafer once again is inspected. Wafers that do not pass this inspection are either scrapped for rework or are removed from the lot.

2.1.5 – Metallization

Metallization is one of the last steps in the fabrication process. It is in this step that the various regions of the device structure are connected to produce a circuit. Aluminum is the most used metal in the this phase, because it satisfies all of the required

constraints, *e.g.* low-resistance electrical contact to the silicon, good adherence to silicon dioxide, economically competitive, etc. The metal is usually deposited by means of vacuum deposition, one wafer at a time. The wafer is placed in a vacuum chamber which is brought down to a very low barometric presure. The aluminum is evaporated by one of several techniques (*e.g.* filament evaporation, electron-beam evaporation, sputtering) and deposits on the wafer. Heating may be required to increase adhesion of the materials.

2.3 – Summary

In this Chapter we discuss at a superficial level the processes involved in transforming a slice of raw silicon into a wafer of integrated circuits. We begin by presenting an overview of the entire manufacturing process (fab, sort, assembly, test) and then describe in more detail the process of fabrication. We describe deposition and epitaxy, oxidation, introduction of impurities, photolithography, and metallization.